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10/692,040	10/22/2003	Srikanth Nagaraja	1488.014US1	6426

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EXAMINER	
WILLIAMS, LAWRENCE B	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/692,040	NAGARAJA, SRIKANTH	
	Examiner	Art Unit	
	Lawrence B. Williams	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-10,12-25,27-34 and 36-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10,12-14,23-34 and 36-40* is/are allowed.

6)☒ Claim(s) *1,8,9,15 and 41* is/are rejected.

7)☒ Claim(s) *3-7 and 17-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1, 3-10, 12-15, 17-34, 36-41 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 15, 41 are rejected under 35 U.S.C. 102(e) as being anticipated by Hadad (US Patent 6,985,432 B1).

(1) With regard to claim 1, Hadad discloses in Fig. 3, a method for synchronizing a receiver clock with a transmitter clock in a communication system, during transmission of a data signal by a transmitter, comprising: obtaining estimates of frequency (AFC; col. 6, lines 35-37) and phase drifts (ASC; col. 6, lines 15-24) between the transmitter and receiver clocks; and synchronizing the receiver clock (NCO, 26; VCO, 23) with the transmitter clock based on the estimated phase and frequency drifts (col. 6, lines 20-24, 44-46); wherein synchronizing the receiver and transmitter clocks comprises: receiving an input pilot signal (Pilot Ext., 27) of a predetermined frequency and phase (col. 8, lines 47-50), by a receiver (Fig. 3) from the transmitter; estimating the frequency (col. 6, lines 35-37) and phase drifts (col. 6, lines 20-24) between the transmitter and the receiver clocks using the input pilot signal (col. 9, lines 22-24);

computing a clock correction parameter based on the phase and frequency drifts; and synchronizing the receiver clock with the transmitter clock based on the clock correction parameter (col. 9, lines 22-24; lines 38-39).

(2) With regard to claim 15, claim 15 discloses substantially the same limitations of claim 1. Therefore a similar rejection applies.

(3) With regard to claim 41, Hadad discloses in Fig. 3, an apparatus for synchronizing local and remote transceiver clock signals in a communicating system, comprising: means to sample an input pilot signal along with a data signal (A/D, FFT, Pilot Ext), wherein the sample input pilot signal is of a predetermined carrier frequency and phase (col. 8, lines 47-50); means to receive the data signal and the input pilot signal, and to estimate a frequency drift between the local and remote transceiver clocks using the input pilot signal (AFC, 5); means to receive the data signal and the input pilot signal, and to estimate a phase drift between the local and remote transceiver clocks using the input pilot signal (ASC, 4); means to receive the estimated phase and frequency drifts, and to compute a clock correction parameter based on the received estimated phase and frequency drifts (ASC, AFC, the AFC, ASC of Hadad both receive the extracted pilot signal and compute a clock correction parameter based on the phase and frequency drifts (col. 6, lines 21-23, lines 35-39)); and means to adjust the local transceiver clock with respect to the input pilot signal, to synchronize the local transceiver clock to the remote transceiver clock, based on the clock correction parameter (VCO, 23, NCO, 20).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

5. Claims 1, 15, 41 are rejected under 35 U.S.C. 102(a) as being anticipated by Keevill et al. (US 2003/0142764 A1).

(1) With regard to claim 1, Keevill et al. discloses in Fig. 13, a method for synchronizing a receiver clock with a transmitter clock in a communication system, during transmission of a data signal by a transmitter, comprising: obtaining estimates of frequency (Frequency error from pilot extract) and phase drifts (Sample rate control from pilot extract) between the transmitter and receiver clocks; and synchronizing the receiver clock (NCO, 140; NCO, 160) with the transmitter clock based on the estimated phase (Sample error update timing) and frequency drifts (Frequency error update timing); wherein synchronizing the receiver and transmitter clocks comprises: receiving an input pilot signal of a predetermined frequency and phase (pg. 2, paragraph 0017; pg. 4, paragraph 0054), by a receiver from the transmitter; estimating the frequency (Fig. 13, frequency error from pilot extract) and phase drifts (Fig. 13, sample rate control from pilot extract) between the transmitter and the receiver clocks using the input pilot signal; computing a clock correction parameter based on the phase and frequency drifts; and synchronizing the receiver clock with the transmitter clock based on the clock correction parameter (Fig. 13, frequency error update and sample error update applied to NCO 150 and 160).

(2) Claim 15 discloses substantially the same limitations of claim 1. Therefore a similar

rejection applies.

(3) With regard to claim 41, Keevill et al. discloses in Fig. 13, an apparatus for synchronizing local and remote transceiver clock signals in a communicating system, comprising: means to sample an input pilot signal along with a data signal (144, Pilot Ext), wherein the sample input pilot signal is of a predetermined carrier frequency and phase (pg. 2, paragraph 0017; pg. 4, paragraph 0054); means to receive the data signal and the input pilot signal, and to estimate a frequency drift between the local and remote transceiver clocks using the input pilot signal (Frequency error from pilot extract); means to receive the data signal and the input pilot signal, and to estimate a phase drift between the local and remote transceiver clocks using the input pilot signal (Sample rate control from pilot extract); means to receive the estimated phase and frequency drifts, and to compute a clock correction parameter based on the received estimated phase and frequency drifts (Frequency error update timing, and Sample error update timing) and means to adjust the local transceiver clock with respect to the input pilot signal, to synchronize the local transceiver clock to the remote transceiver clock, based on the clock correction parameter (NCO, 150, 160).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Hadad (US Patent 6,985,432 B1) as applied to claim 1 above, and further in view of Sawahashi et al. (US Patent 5,694,388).

Claim 8 inherits all limitations of claim 1 above. As noted above, Hadad discloses all limitations of claim 1. Hadad does not explictly teach wherein estimating the phase drift comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift by using the estimate of the phase of the input pilot signal and the estimated reference phase.

However, Sawahashi et al. teaches wherein estimating a phase drift (error) comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift (error) by using the estimate of the phase of the input pilot signal and the estimated reference phase (col. 24, line 61-col. 25, line 3).

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Sawahashi et al. to obtain an accurate measure of phase drift/error in the signal.

(2) With regard to claim 9, Hadad also discloses in Fig. 3, wherein synchronizing the receiver clock with the transmitter clock further comprises: synchronizing the receiver clock with the transmitter clock by correcting for the phase drift (ASC) substantially after correcting for the frequency drift (AFC). Hadad discloses the AFC being applied well before the ASC since it is well known in the art that frequency drift results in phase drift.

8. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Keevill et al. (US 2003/0142764 A1) as applied to claim 1 above, and further in view of Sawahashi et al. (US Patent 5,694,388).

Claim 8 inherits all limitations of claim 1 above. As noted above, Keevill et al. discloses all limitations of claim 1. Keevill et al. does not explictly teach wherein estimating the phase drift comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift by using the estimate of the phase of the input pilot signal and the estimated reference phase.

However, Sawahashi et al. teaches wherein estimating a phase drift (error) comprises: estimating a reference phase; estimating the phase of the input pilot signal; and obtaining the phase drift (error) by using the estimate of the phase of the input pilot signal and the estimated reference phase (col. 24, line 61-col. 25, line 3).

It would have been obvious to one skilled in the art at the time of the invention to incorporate the teachings of Sawahashi et al. to obtain an accurate measure of phase drift/error in the signal.

(2) With regard to claim 9, Keevill et al. also discloses in Fig. 13, wherein synchronizing the receiver clock with the transmitter clock further comprises: synchronizing the receiver clock with the transmitter clock by correcting for the phase drift (NCO, 160) substantially after correcting for the frequency drift (NCO, 150). Keevill et al. discloses the frequency error (drift) update timing being applied well before the sample update timing (phase drift) since it is well known in the art that frequency drift results in phase drift.

Allowable Subject Matter

9. Claims 10, 12-14, 22-34, 36-40 are allowed.

10. Claims 3-7, 17-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. The following is an examiner's statement of reasons for allowance: The instant application discloses a method for synchronizing a receiver clock with a transmitter clock. A search of prior art records has failed to teach or suggest alone or in combination a method for synchronizing a receiver clock with a transmitter clock:

"wherein synchronizing the receiver and transmitter clocks comprises: obtaining a window length from an experimental knowledge base; forming a window using the window length; estimating the frequency and phase drifts between the transmitter and the receiver clocks using an input pilot signal and the window; computing a clock correction parameter based on the phase and frequency drift estimates; synchronizing the receiver and transmitter based on the clock correction parameter; and repeating the estimating, computing and synchronizing steps for a next window" as disclosed in claim 10.

Nor does the prior art teach:

"a clock correction module in a local receiver to synchronize a local receiver clock, in the local receiver, with a remote transmitter clock, in a remote transmitter, in a multi-carrier communication system, while transmitting a data signal by the remote transmitter, comprising: a

data sampler to sample an input pilot signal of a predetermined carrier frequency and phase; a frequency drift estimator, coupled to the data sampler, to receive the data signal along with the input pilot signal, and to estimate a frequency drift between the receiver and transmitter clocks using the input pilot signal; a phase drift estimator, coupled to the data sampler and the frequency drift estimator, to receive the data signal along with the input pilot signal, and to estimate a phase drift between the receiver and transmitter clocks using the input pilot signal; an analyzer, coupled to the frequency drift estimator and the phase drift estimator, to receive the estimated phase and frequency drifts, and to compute a clock correction parameter based on the received estimated phase and frequency drifts; and a synchronizing block, coupled to the analyzer, to receive the clock correction parameter, and to adjust the receiver clock to synchronize the receiver clock with the transmitter clock based on the clock correction parameter" as disclosed in claim 23.

"an apparatus for synchronizing local and remote transceiver clock signals in a communicating system, comprising: a data sampler to sample an input pilot signal along with a data signal, wherein the input pilot signal is of a predetermined carrier frequency and phase; a frequency drift estimator, coupled to the data sampler, to receive the data signal and the input pilot signal, and to estimate a frequency drift between the local and remote transceiver clocks using the input pilot signal; a phase drill estimator, coupled to the data sampler and the frequency drill estimator, to receive the data signal and the input pilot signal, and to estimate a phase drift between the local and remote transceiver clocks using the input pilot signal; an analyzer, coupled to the frequency drill estimator and the phase drift estimator, to receive the estimated phase and frequency drills, and to compute a clock correction parameter based on the received estimated

phase and frequency drifts; and a synchronizing block, coupled to the analyzer, to receive the clock correction parameter, and to adjust the local transceiver clock with respect to the input pilot signal, to synchronize the local transceiver clock to the remote transceiver clock, based on the clock correction parameter" as disclosed in claim 30.

"an article comprising a computer-readable medium which stores computer-executable instructions, the instructions causing a computer to: receive an input pilot signal, of a predetermined frequency, amplitude, and signal phase, by a local receiver clock from a remote transmitter; estimate the frequency and phase drifts between a remote transmitter clock in the remote transmitter and the receiver clock using the input pilot signal; compute a clock correction parameter based on the phase and frequency drift estimates; synchronize the local receiver clock with the remote transmitter clock based on the clock correction parameter; estimate a window length using the input pilot signal; and repeat the estimate of the frequency and phase drifts, the computation of the clock correction parameter and the synchronization of the local receiver clock and the remote transmitter clock steps for the window length" as disclosed in claim 34.

"a computer system for synchronizing clock signals in a communication system used in a multi-carrier system, comprising: a bus; a processor coupled to the bus; a memory coupled to the processor; a data sampler to sample an input pilot signal of a predetermined carrier frequency nd phase; a frequency drift estimator, coupled to the data sampler, to receive a data signal along with the input pilot signal, and to estimate a frequency drift between receiver and transmitter clocks using the input pilot signal; a phase drift estimator, coupled to the data sampler and the frequency drift estimator, to receive the data signal along with the input pilot signal, and to

estimate a phase drift between the receiver and transmitter clocks using the input pilot signal; an analyzer, coupled to the frequency drift estimator and the phase drift estimator, to receive the estimated phase and frequency drifts, and to compute a clock correction parameter based on the received estimated phase and frequency drifts; and a synchronizing block, coupled to the analyzer, to receive the clock correction parameter, and to adjust the receiver clock to synchronize a receiver clock with a transmitter clock based on the clock correction parameter" as disclosed in claim 38.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.) Nakahara et al. disclosed in US Patent 7,027,464 B1 OFDM Signal Transmission Scheme, And OFDM Signal Transmitter/Receiver.

b.) Nakahara et al. disclosed in US 2006/0104195 A1 OFDM Signal Transmission Scheme, And OFDM Signal Transmitter/Receiver.

c.) Morgan et al. discloses in US 2002/0186802 A1 Apparatus And Method For Adaptively Adjusting A timing Loop.

d.) Bennett et al. discloses in US Patent 6,701,133 B1 Apparatus For And Method Of Synchronising Oscillators Within A Data Communication System.

e.) Hadad discloses in US 2005/0207334 A1 OFDM Communication Channel.

f.) Wu et al. discloses in US Patent 6,370,188 B1 Phase And Frequency Offset Compensation In A Telecommunications Receiver.

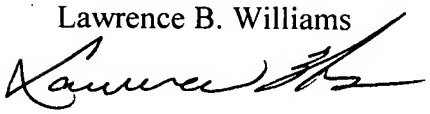
g.) Kumagai et al. discloses in US Patent 7,058,002 B2 OFDM Packet Communication Receiver.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lawrence B Williams whose telephone number is 571-272-3037. The examiner can normally be reached on Monday-Friday (8:00-6:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ghayour Mohammad can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lawrence B. Williams



lbw
August 4, 2007

MOHAMMED GHAYOUR
SUPERVISORY PATENT EXAMINER